In the Claims:

Please amend claims 1, 2, 9, and 12. Please cancel claim 10. Please add new claim 21.

The claims are as follows:

1. (Currently Amended) An electronic circuit, comprising:

a memory cell array; ~~including~~

a sense amplifier self-timed decode circuit adapted to set a base read time delay of said memory cell array; [[anda] and

a read delay adjustment circuit coupled to said memory cell array, said read delay adjustment circuit adapted to adjust said base read time delay of said memory array based on an operating frequency of said memory cell array.

2. (Currently Amended) ~~The circuit of claim 1, wherein said read delay adjustment circuit~~ includes An electronic circuit, comprising:

a memory cell array;

a sense amplifier self-timed decode circuit adapted to set a base read time delay of said memory cell array;

a read delay adjustment circuit coupled to said memory cell array, said read delay adjustment circuit adapted to adjust said base read time delay of said memory array based on an operating frequency of said memory cell array;

a sense amplifier delay circuit coupled between said sense amplifier self-timed decode circuit and said memory cell array, said sense amplifier delay circuit adapted to control an

amount of delay time added to said base read time delay in response to a margin select signal; and

a read margin adjustment circuit coupled to said sense amplifier delay circuit, said read margin adjustment circuit adapted to generate said margin select signal.

3. (Previously Presented) The circuit of claim 2, wherein said read margin adjustment circuit includes:

a microprocessor adapted to execute a load instruction issued in response to a change of value of said operating frequency of said microprocessor and of said memory cell array and to store data associated with said load instruction in a register, an output of said register coupled to said sense amplifier delay circuit.

4. (Previously Presented) The circuit of claim 2, wherein said read margin adjustment circuit includes:

a microprocessor adapted to generate a frequency select signal to select an operating frequency of said microprocessor and said operating frequency of said memory cell array; and

a register adapted to store said frequency select signal, an output of said register coupled to said sense amplifier delay circuit.

5. (Previously Presented) The circuit of claim 2, wherein said read margin adjustment circuit includes:

a frequency selection circuit adapted to generate said operating frequency of said memory cell array from an internal frequency generation circuit or from an external clock signal; and

a frequency detector coupled between said frequency selection circuit and said sense amplifier delay circuit.

6. (Previously Presented) The circuit of claim 2, further including one or more programmable fuses coupled to said sense amplifier delay circuit, said sense amplifier delay circuit adapted to set an initial time adjustment to said base read time delay based on a state of said one or more fuses.

7. (Previously Presented) The circuit of claim 6, wherein said sense amplifier delay circuit is adapted to override said initial time adjustment based on said margin select signal.

8. (Previously Presented) The circuit of claim 1, further including;

a microprocessor; and

said memory cell array is a cache memory coupled to said microprocessor.

9. (Currently Amended) ~~The circuit of claim 1,~~ An electronic circuit, comprising:

a memory cell array;

a sense amplifier self-timed decode circuit adapted to set a base read time delay of said memory cell array;

a read delay adjustment circuit coupled to said memory cell array, said read delay adjustment circuit adapted to adjust said base read time delay of said memory array based on an operating frequency of said memory cell array; and

wherein said base read time delay is based on a first operating frequency and a corresponding first operating voltage, and time adjustment to said base read time delay is based on a second operating frequency and a corresponding second operating voltage.

10. (Canceled)

11. (Currently Amended) The method of claim [[10]] 21, wherein said base read time delay is based on high performance operation of said self-timed memory array at a maximum operating frequency and at a corresponding maximum voltage and said self-timed memory array is adapted to add additional read time delay in low power operation wherein said low power operation, said memory is adapted to operate at an operating frequency that is less than said maximum operating frequency and a corresponding operating voltage is less than said maximum operating voltage.

12. (Currently Amended) A method for adjusting the read margin of a self-timed memory cell array, comprising:

providing a memory cell array; ~~including~~

providing a sense amplifier self-timed decode circuit for setting a base read time delay of said memory cell array; and

providing a read delay adjustment circuit coupled to said memory cell array, said read delay adjustment circuit for adjusting said base read time delay of said memory array based on an operating frequency of said memory cell array.

13. (Previously Presented) The method of claim 12, wherein said read delay adjustment circuit includes:

a sense amplifier delay circuit coupled between said sense amplifier self-timed decode circuit and said memory cell array, said sense amplifier delay circuit for controlling an amount of delay time added to said base read time delay in response to a margin select signal; and

a read margin adjustment circuit coupled to said sense amplifier delay circuit, said read margin adjustment circuit for generating said margin select signal.

14. (Previously Presented) The method of claim 13, wherein said read margin adjustment circuit includes:

a microprocessor for executing a load instruction issued in response to a change of value of said operating frequency of said microprocessor and of said memory cell array and for storing data associated with said load instruction in a register, an output of said register coupled to said sense amplifier delay circuit; and

further including, when said operating frequency is to be decreased, sequentially decreasing said operating frequency, issuing said margin select signal and decreasing said operating voltage in the order recited and when said operating frequency is to be increased, sequentially increasing said operating voltage, issuing said margin select signal and increasing said operating voltage in the order recited.

15. (Previously Presented) The method of claim 13, wherein said read margin adjustment circuit includes:

a microprocessor for generating a frequency select signal for selecting an operating frequency of said microprocessor and said operating frequency of said memory cell array;

a register for storing said frequency select signal, an output of said register coupled to said sense amplifier delay circuit; and

further including, when said operating frequency is to be decreased, sequentially decreasing said operating frequency, issuing said margin select signal and decreasing said operating voltage in the order recited and when said operating frequency is to be increased, sequentially increasing said operating voltage, issuing said margin select signal and increasing said operating voltage in the order recited.

16. (Previously Presented) The method of claim 13, wherein said read margin adjustment circuit includes:

a frequency selection circuit for generating said operating frequency of said memory cell array from an internal frequency generation circuit or from an external clock signal; and

a frequency detector coupled between said frequency selection circuit and said sense amplifier delay circuit.

17. (Previously Presented) The method of claim 13, further including:

providing one or more programmable fuses coupled to said sense amplifier delay circuit, said sense amplifier delay circuit for setting an initial time adjustment to said base read time delay based on a state of said one or more fuses.

18. (Previously Presented) The method of claim 17, wherein said sense amplifier delay circuit is adapted to override said initial time adjustment based on said margin select signal.

19. (Previously Presented) The method of claim 12, further including;

providing a microprocessor; and

wherein said memory cell array is a cache memory coupled to said microprocessor.

20. (Previously Presented) The method of claim 12, wherein said base read time delay is based on a first operating frequency and a corresponding first operating voltage, and time adjustment to said base read time delay is based on a second operating frequency and a corresponding second operating voltage.

21. (New) A method for adjusting the read margin of a self-timed memory, comprising:

providing said self-timed memory, said self-timed memory adapted to generate a base read time delay; and

providing said self-timed memory with a read delay adjustment circuit, said read delay adjustment circuit adapted to adjust said base read time delay in order to increase or decrease the read margin of said self-timed memory.